REMARKS

1. Request for Continued Examination:

The Applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

2. Amendments to the specification:

The paragraph 0022 has been amended by inserting a space in the term "Fig.8of". No new matter is introduced. Allowance of the amendments is respectfully requested.

3. Response to the rejection of claims 1-6 under 35 U.S.C. 103(a):

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beddingfield, US Patent 5,977,632 in view of Dass et al., US Patent 6,162,652 and further in view of Applicant's Admitted Prior Art (AAPA).

Beddingfield discloses providing a semiconductor wafer (10), which comprises a substrate (10), an integrated circuit (not shown), and at least one bump pad (12) formed on the substrate and electrically connected with the integrated circuit; forming a first dielectric layer (16) on a surface of the bump pad; performing an etching process to form a contact hole in the first dielectric layer (figure 1) and to expose a portion of the bump pad (12); forming a second

dielectric layer (18) on a surface of the semiconductor wafer outside of the contact hole, performing an under bump metallurgy (UBM) process so as to form a metal layer (24) on a surface of the contact hole; forming a solder bump (26) on the metal layer corresponding to the contact hole; and performing a connection process to complete connection of the semiconductor wafer and a packaging board (figure 7). Please see figures 1-7 and discussion on column 2, line 35 to column 4, and line 35. Also in regards to claim 6 wherein the second dielectric layer is composed of insulating materials, such as benocyclobutene (BCB), polyimide (PI), and BCB+PI (column 3, lines 5 to 15).

Beddingfield is applied supra but lacks the anticipation of wherein the circuit probing and an laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. Dass discloses circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. See figure 17 and discussion on column 7, line 45 to column 8, line 30. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to circuit probing and a laser repair process are preformed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump as taught by Dass et al, because by testing after bumping

and before laser repair the throughput is increased.

In regards to claims 2-4, Beddingfield is applied supra but lacks the anticipation wherein the semiconductor wafer further comprises a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key. AAPA discloses a semiconductor wafer 10 comprises a substrate 12, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 12 further comprises a bump pad 14, a plurality of fuses 16, and an alignment key 18. The bump pad 14 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 14. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to form a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key as taught by AAPA in view of the primary reference of Beddingfield, because the alignment key provides a means for visual inspection and the fuse provide electrical connection for probe testing.

Response:

Claim 1 is amended to introduce the limitation such

as "fuses" to overcome this rejection. The amendments in claim 1 are disclosed in paragraph 0021 of the specification. No new matter is introduced by these amendments.

The amended claim 1 of the present invention discloses a solder bump structure and a laser repair process, and wherein a circuit probing process through the solder bump and a laser repair process to cut off portions of fuses are performed after the formation of the solder bump. The cited references including Beddingfield and Dass do not teach the inventive concept of "performing a circuit probing process through the solder bump and a **laser repair process** to cut off portions of fuses after the formation of the solder bump". Beddingfield teaches a bump structure without any fuses thereon. Dass teaches a method of testing a bumped wafer, and no fuses are shown in the bumped wafer. Because Beddingfield and Dass never disclose fuses on the bumped wafer, no laser repair process is possibly suggested by them to cut off the fuses according to the circuit probing test.

From the aforementioned reasons, the Applicant believes that one of ordinary skill cannot combine the inventions of Beddingfield and Dass to accomplish the present application. Reconsideration of the amended claim 1 is politely requested.

As claims 2-4 and 6 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of claims 2-4 and 6 is

therefore requested.

4. Response to the rejection of claims 7-9 under 35 U.S.C. 103(a):

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loo et al, US Patent 6,118,180 in view of Dass et al, US Patent 6,162,652 and further in view of Applicant's Admitted Prior Art (AAPA).

Loo discloses providing a semiconductor wafer (400), which comprises a substrate, an integrated circuit, and at least one bump pad (402) formed on the substrate and electrically connected with the integrated circuit; forming a dielectric layer (406) on a surface of the bump pad; performing an etching process to form a contact hole in the dielectric layer (figure 6) and to expose a portion of the bump pad; performing an under bump metallurgy (UBM) process so as to form a metal layer (408) on a surface of the contact hole; forming a solder bump (412) on the metal layer corresponding to the contact hole; and performing a connection process to complete connection of the semiconductor wafer and a packaging board. See figures 3-6 and discussion on column 5, line 30 to column 8, line 15.

Loo is applied supra but lacks the anticipation of wherein the circuit probing and a laser repair process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. Dass discloses circuit probing and a laser repair

process are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump. See figure 17 and discussion on column 7, line 45 to column 8, line 30. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention to circuit probing and a laser repair are performed after the formation of the solder bump, and a probing tip is used to perform the circuit probing process by electrically connecting with the solder bump as taught by Dass et al, because by testing after bumping and before laser repair the throughput is increased.

In regards to claims 8 and 9, Loo is applied supra but lacks the anticipation wherein the semiconductor wafer further comprises a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key. AAPA discloses a semiconductor wafer 10 comprises a substrate 12, which has an integrated circuit region (not shown) comprising an embedded memory array formed on its surface. The surface of the substrate 12 further comprises a bump pad 14, a plurality of fuses 16, and an alignment key 18. The bump pad 14 is electrically connected with the integrated circuit region. Therefore, after completing a subsequent packaging process, the integrated circuit is able to electrically connect to an external circuit through the bump pad 14. In view of this disclosure it would have been obvious to one of ordinary skill in the art at the time of invention

to form a plurality of fuses electrically connected with the integrated circuit; at least one alignment key; and a silicon oxide layer formed on a surface of the fuses and the alignment key as taught by AAPA in view of the primary reference of Loo, because the alignment key provides a means for visual inspection and the fuse provides electrical connection for probe testing.

Response:

Claim 7 is amended to introduce the limitation such as "fuses" to overcome this rejection. The amendments in claim 7 are disclosed in paragraph 0022 of the specification. No new matter is introduced by these amendments.

The amended claim 7 of the present invention discloses a solder bump structure and a laser repair process, and wherein a circuit probing process through the solder bump and a laser repair process to cut off portions of fuses are performed after the formation of the solder bump. The cited references including Loo and Dass do not teach the inventive concept of "performing a circuit probing process through the solder bump and a **laser repair process** to cut off portions of fuses after the formation of the solder bump". Because Loo and Dass never disclose fuses on the bumped wafer, no laser repair process is possibly suggested by them to cut off the fuses according to the circuit probing test.

From the aforementioned reasons, the Applicant believes that one of ordinary skill cannot combine the inventions of Loo and Dass to accomplish the present application. Reconsideration of the amended claim 7 is politely requested.

As claims 8-9 are dependent upon the amended claim 7, they should be allowed if the amended claim 7 is allowed. Reconsideration of claims 8-9 is therefore requested.

5. Introduction to new claim 11:

Claim 11 is added to emphasize the outstanding feature of the present invention. The limitations of claim 11 are entirely supported by the disclosure, and specifically, by paragraph 0019-0024 on pages 5-6 of the specification, for instance. The outstanding feature stated in new claim 11 includes performing a circuit probing process through the solder bump and a laser repair process to cut off portions of the fuses **after the formation of the solder bump and the second dielectric layer**, so as to prevent the laser repair process from resulting voids in the second dielectric layer. Claim 11 is believed patentably different from all the cited prior arts. Consideration of new claim 11 is politely requested.

Sincerely,

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